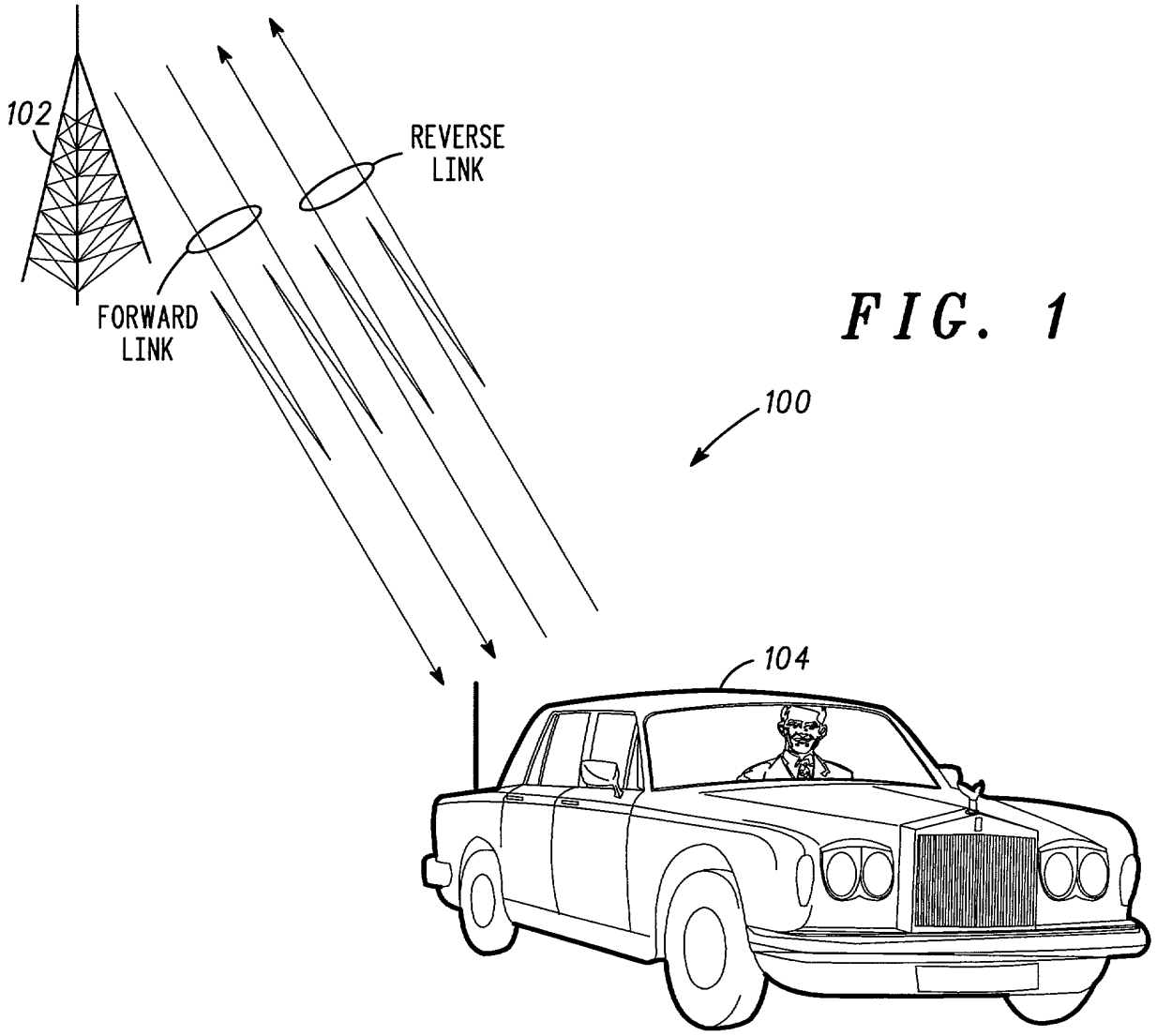
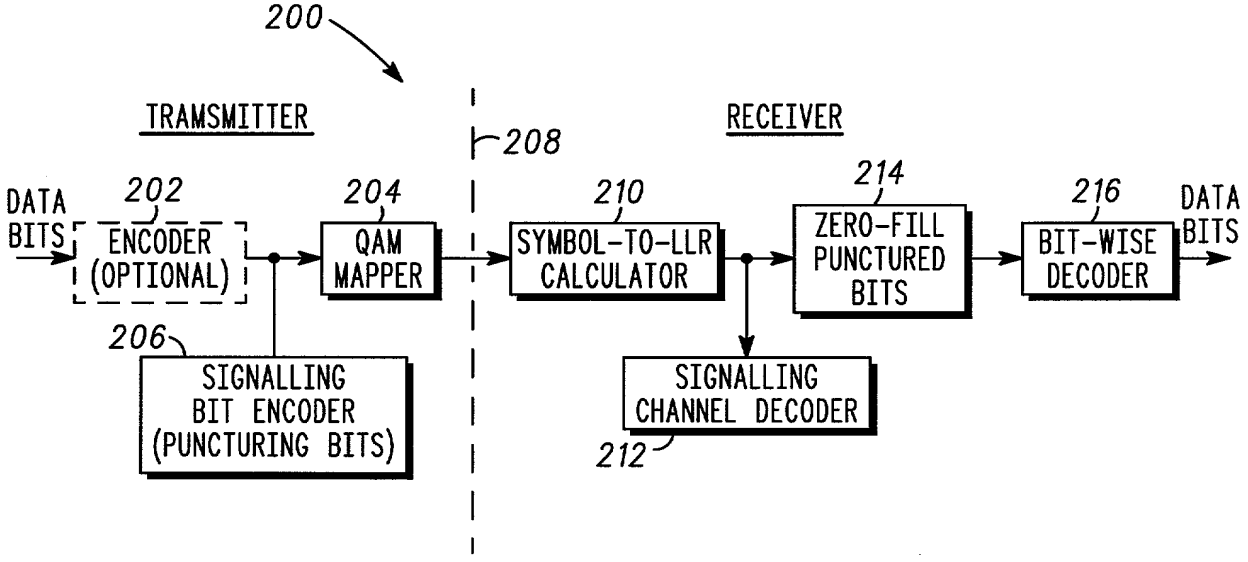

102
REVERSE LINK
FORWARD LINK
100
104

FIG. 1

FIG. 2


200
TRAMSMITTER
RECEIVER
208
DATA BITS
202
ENCODER (OPTIONAL)
204
QAM MAPPER
206
SIGNALLING BIT ENCODER (PUNCTURING BITS)
210
SYMBOL-TO-LLR CALCULATOR
212
SIGNALLING CHANNEL DECODER
214
ZERO-FILL PUNCTURED BITS
216
BIT-WISE DECODER
DATA BITS

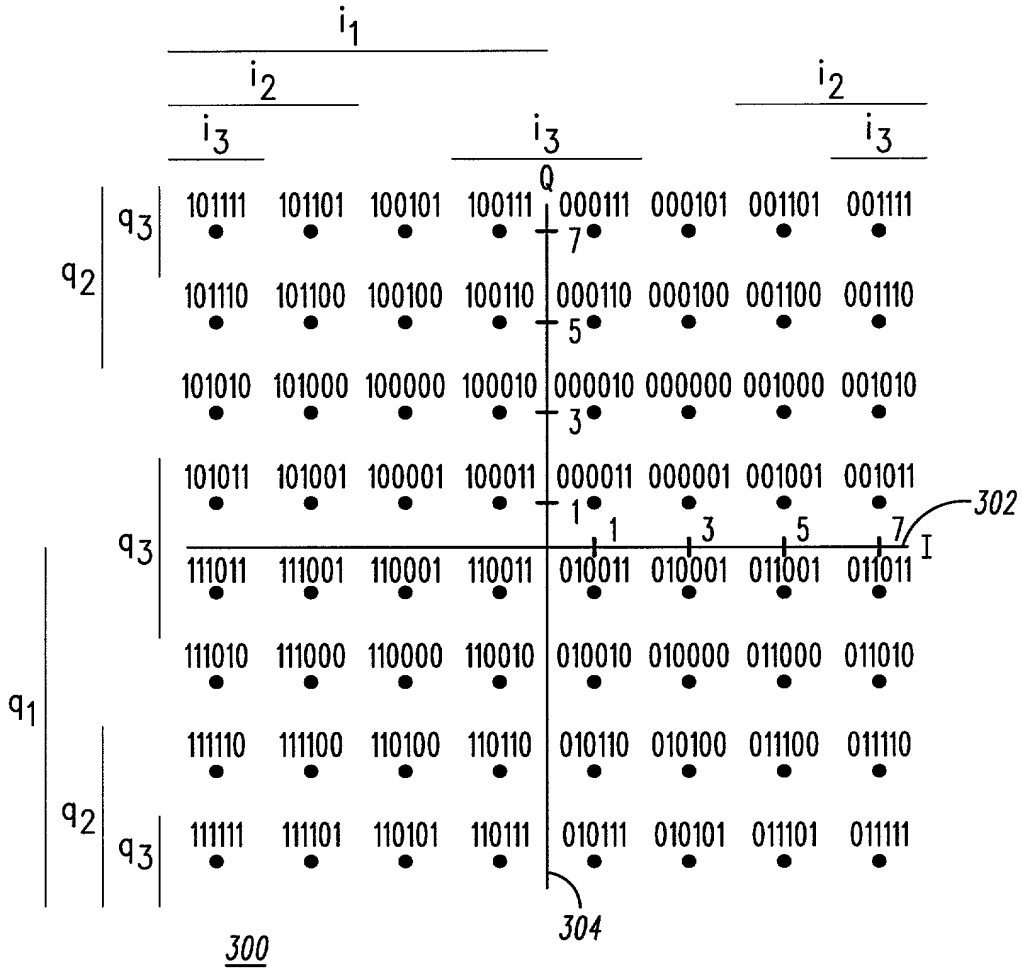

i1
i2
i2
i3
i3
i3
Q
I
q1
q2
q2
q3
q3
q3
101111 101101 100101 100111 000111 000101 001101 001111
101110 101100 100100 100110 000110 000100 001100 001110
101010 101000 100000 100010 000010 000000 001000 001010
101011 101001 100001 100011 000011 000001 001001 001011
111011 111001 110001 110011 010011 010001 011001 011011
111010 111000 110000 110010 010010 010000 011000 011010
111110 111100 110100 110110 010110 010100 011100 011110
111111 111101 110101 110111 010111 010101 011101 011111
7
5
3
1
1
3
5
7
302
304
300

FIG. 3

BIT POSITION	DEPENDENCY ON OTHER BITS	LLR
BIT b_0	NONE	$\pm 4D^2$
BIT b_1	NONE	$\pm 4D^2$
BIT b_2	BIT b_0=1	$\pm 16D^2$
	BIT b_0=0	$\pm 4D^2$
BIT b_3	BIT b_1=1	$\pm 16D^2$
	BIT b_1=0	$\pm 4D^2$
BIT b_4	BIT b_2=1, BIT b_0=1	$\pm 64D^2$
	BIT b_2=1, BIT b_0=0	$\pm 36D^2$
	BIT b_2=0, BIT b_0=0	$\pm 16D^2$
	BIT b_2=0, BIT b_0=1	$\pm 4D^2$
BIT b_5	BIT b_3=1, BIT b_1=1	$\pm 64D^2$
	BIT b_3=1, BIT b_1=0	$\pm 36D^2$
	BIT b_3=0, BIT b_1=0	$\pm 16D^2$
	BIT b_3=0, BIT b_1=1	$\pm 4D^2$

FIG. 4

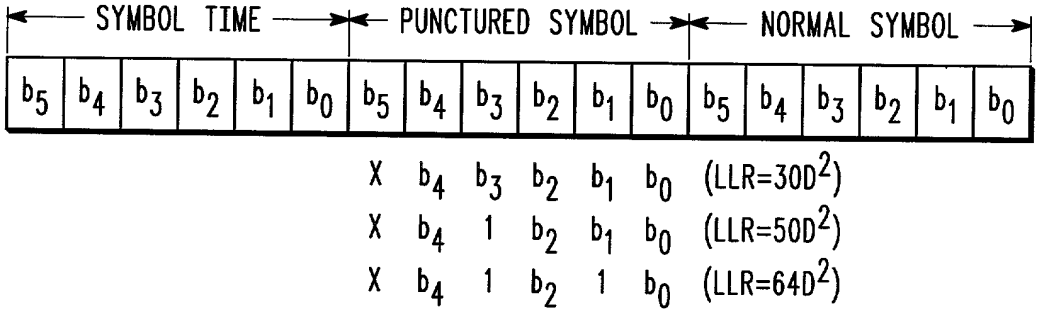


FIG. 5